PATENT ABSTRACTS OF JAPAN

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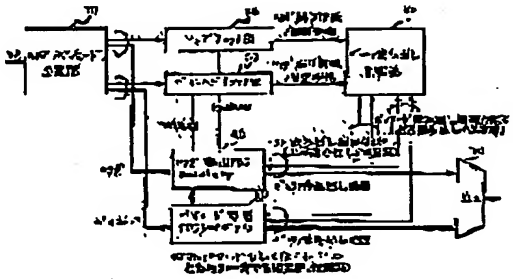
(54) PARALLEL-TYPE ERROR DETECTION CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the delay of a cell and to improve processing efficiency by error-detecting in parallel and storing a header and a payload obtained by separating an input cell, performing read from a storage means which performs an FEC processing, when error correction is required and performing synthesis and output.
SOLUTION: A separation part 10 separates the header and payload of an ATM cell. check parts 20 and 30 check errors and FEC work buffers 50 and 60 perform storage tentatively. When error correction is required, the check parts 20 and 30 instruct the FEC processing t the buffers 50 and 60, and each error information is r ported to a buffer read control part 40. The control part 40 makes the buffers 50 and 60 abandon the cell for which the error is detected in a CRC processing after the FEC processing at the time of read and perform update for each cell, based on the error information. An MUX part 7 synthesizes and outputs the header and the payload outputted by the buffers 50 and 60 after the CRC/FEC processings. Thus, error, error detection and correction processing delay time is reduced.



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